Implementation Of Built-In Self-Test Architecture For UART Using VHDL

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ABSTRACT: The Universal Asynchronous Receiver Transmitter (UART) is an asynchronous serial communication interface that many peripheral devices and central processing units use to allow for the cheap and easy transfer of data over short distances. Its full-duplex communication features make it indispensable in embedded systems, digital communication applications, and industrial control. As more and more features are packed onto a single chip in today's electronics, compact, dependable, and well-tested UART solutions are becoming crucial. This paper incorporates a status register and Built-In Self-Test (BIST) architecture into the UART design to enhance system reliability and streamline manufacturing process testing. By eliminating costly external testing instruments, the BIST module enhances on-chip testing. This results in improved fault detection and shorter testing times. Data connection reliability and accuracy are ensured by the status register, which provides real-time information on transmission, reception, and error conditions. The Built-In Self-Test (BIST) architecture that has been recommended reduces switching during test patterns by employing Single Input Change (SIC) test vectors, which contributes to its low power consumption. The counter and Gray code generator outputs are XORed with the LP-LFSR seed to generate these vectors. This approach significantly reduces power consumption during testing while simultaneously enhancing fault coverage. The following tools are employed for simulation and synthesis after the design is generated in VHDL: Xilinx ISE Development Suite 14.4. The subsequent phase involves configuring it on an FPGA system. A status register and a Built-In Self-Test (BIST) module are included in the 8-bit UART. Modern designs are able to benefit from improved serial communication, dependable fault detection, less power consumption during testing, and easier testing as a result of advancements in embedded and communication systems. This academic work employs a variety of terms, including Asynchronous Serial Communication, Fault Detection, Status Register, VHDL, and Low-Power Testing (LP-LFSR).

Keywords: *UART, Asynchronous Serial Communication, Built-In Self-Test (BIST), Status Register, VHDL, FPGA, Low-Power Testing, LP-LFSR, Design for Testability (DFT), Fault Detection.*

I. INTRODUCTION

The electronics industry has been transformed by Very Large-Scale Integration (VLSI) technology, which enables the integration of millions of transistors onto a single semiconductor chip. The development of small, powerful electronics that provide adequate performance while using less power has been facilitated by modern manufacturing techniques, advancements in semiconductor technology, and new circuit

design approaches. Very large-scale integration (VLSI) technology is a critical component of contemporary electronic devices, including computers, phones, and cars.

The demand for embedded devices that can be easily transported, connection speeds, and the processing of data at a faster rate is creating a growing need for digital communication interfaces that are both efficient and stable. Because of its ease of use, low hardware cost, and simple configuration, the Universal Asynchronous Receiver Transmitter (UART) protocol is widely used for serial communication between devices. Without requiring a shared clock, UART enables asynchronous full-duplex communication among processors, sensors, microcontrollers, and other peripherals. FPGAs have a wide range of potential applications, such as embedded systems, medical devices, IoT devices, and communication platforms.

The complexity of very large scale integration (VLSI) systems can make it challenging to test for reliability and accuracy. Reliable testing methodologies are essential due to the potential detrimental effects of age, operational errors, and manufacturing flaws on system performance. Design for Testability (DFT) methodologies, such as Built-In Self-Test (BIST), are gaining popularity in order to reduce testing costs, reduce dependence on external testing equipment, and increase fault coverage. BIST enables the circuit to independently generate test patterns and evaluate the results, thereby reducing testing durations and improving system reliability.

This article examines an 8-bit UART that incorporates a BIST architecture and a status register. The proposed design employs Gray code generation, Single Input Change (SIC) test patterns, and Low-Power Linear Feedback Shift Register (LP-LFSR) to minimize switching and power consumption during testing without compromising fault coverage. The Xilinx ISE Design Suite 14.4 is employed to synthesize and simulate the design, which is expressed in VHDL. An FPGA platform is utilized to execute all operations. The proposed design is compatible with contemporary embedded communication systems that are based on very large scale integration (VLSI) and provide a low-power testing solution. Two potential outcomes are enhanced communication reliability and problem-solving abilities.

II. BIST ARCHITECTURE

The Built-In Self-Test (BIST) architecture is a testing methodology that is effective in eliminating the need for supplementary testing tools. It is indispensable for the proper operation of digital circuits. The architecture of the Built-In Self-Test (BIST) is illustrated in Figure 1. The Test Response Analyzer (TRA), Circuit Under Test (CUT), Linear Feedback Shift Register (LFSR), and Test Pattern Generator (TPG) comprise the testing system's components. These components collaborate to generate test patterns, integrate them into the circuit, assess the outcomes, and identify issues.

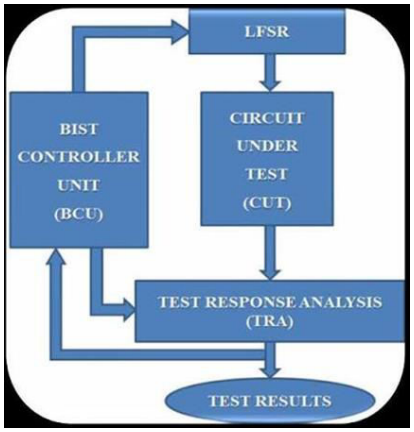

Figure 1: Block Diagram of BIST Architecture

The LFSR generates test sequences that appear to be randomly selected for the CUE. The CUT is capable of displaying digital circuits that include memory modules, FPGA-based hardware configurations, or UARTs. Transition, bridging, and stuck-at faults are among the errors that can be identified through test patterns that involve the functional channels of the circuit.

The BIST Controller supervises the interoperability of all testing modules, the management of test sequences, and the configuration of LFSRs. While testing is in progress, it supervises all aspects. It guarantees that the CUT receives the appropriate test vectors in the correct sequence at the appropriate time.

The Test Response Analyzer (TRA) is employed to acquire the CUT results. The TRA compares the measured responses to the reference signatures to verify the circuit's functionality. Whenever a discrepancy is identified, the system records the pertinent error details.

The TRA is responsible for determining the success or failure of the CUT's self-test. The BIST architecture in UART applications compares the data bits sent and received to verify the proper operation of the transmitter and receiver. It is feasible to identify and preserve defects for subsequent assessment. Examine the simulation waveforms and FPGA implementation outcomes to confirm the overall efficacy of the BIST-enabled design.

III. UART ARCHITECTURE

Through a hardware component known as a Universal Asynchronous Receiver/Transmitter (UART), digital devices are capable of transmitting and receiving asynchronous serial data. While transmitting data from a processor or controller, it converts it from parallel to serial, and upon receipt, it converts it back to parallel. UART communication does not require an external clock signal for synchronization as a result of the use of start bits, stop bits, and an optional parity bit.

The TX and RX functional blocks are the focal point of the majority of UART designs. The transmitter adds the requisite start and stop bits to transmit data serially over the TX line after receiving parallel data from the system and storing it in the transmit buffer. Subsequently, the receiver validates the data format, eliminates the start and stop bits, and stores the parallel data extracted in the receive buffer after acquiring serial data on the RX line.

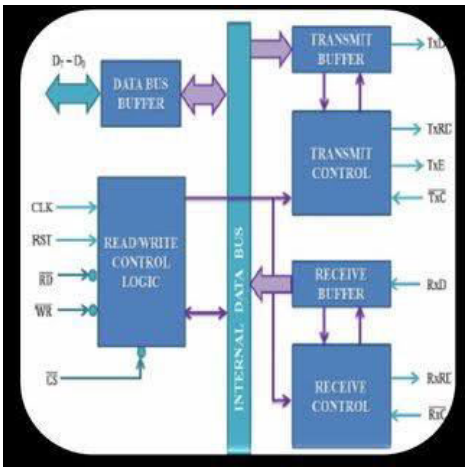

Figure 2: Block diagram of UART Architecture

The ability to generate baud rates, a transmitter, receiver, data buffers, control registers, status registers, and a user-address translation register (UART) all collaborate to maintain the stability of the connection. The control and status registers monitor and adjust the communication parameters, while the baud rate generator establishes the transmission

speed. Buffered read and write operations enable the processor and the UART module to transmit data in a seamless manner.

UART is a widely used component in embedded systems, FPGA designs, microcontrollers, and serial communication interfaces due to its dependable data transmission over short to medium distances, simple hardware implementation, and low cost.

IV. UART COMMUNICATION

Universal Asynchronous Receiver/Transmitter (UART) communication is a prevalent form of asynchronous serial communication that enables two digital devices to exchange data without sharing a clock signal. Additional signaling between the UART modules is unnecessary; only the TX and RX lines are required for initialization. In order to transmit and receive serial data, it is necessary to connect the TX pin of the sending UART to the RX pin of the receiving UART.

Data transmissions are conducted in parallel between the UART and the host device, which may be a microprocessor, microcontroller, or field-programmable gate array (FPGA). The parallel data is converted into a serial bit stream by adding a start bit, a parity bit (if desired), and one or more stop bits prior to transmission over the TX line. On the other side, the UART looks for the start bit, then sequentially gets the serial data bits, checks the parity (if enabled), discards the stop bit or bits, and finally puts together the original parallel data to process further.

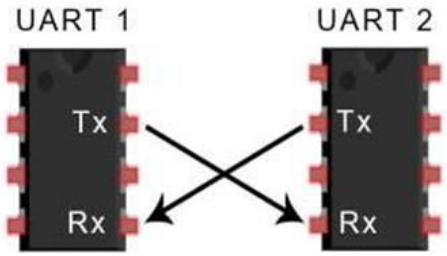

Figure 3: UART Communication

A shift register is a critical component of any UART, as it is responsible for converting data from a parallel to a serial format. The shift register acquires and stores new bits in a register as the byte is being completed. It emits signals gradually. In comparison to parallel communication, this serial transmission method significantly reduces the number of communication lines necessary. This leads to a device that is more energy-efficient, less expensive, and simpler to operate.

UART communication is employed by a diverse array of computer peripherals, sensors, microcontrollers, FPGA implementations, and embedded systems due to its simplicity, reliability, and lack of configuration complexity. Point-to-point communication is an appropriate solution for applications that require dependable serial data transmission at moderate data rates.

V. REVIEW OF LITERATURE

K. Gupta et al. (2020): The authors developed and executed an architecture for high-speed UART to guarantee dependable serial communication in digital systems. The design aimed to achieve maximum transmission speed and optimal hardware complexity. The FPGA implementation was implemented to guarantee the design's functionality. The simulations and hardware tests demonstrated a consistent connection with

minimal latency. This UART is an excellent option for the rapid transmission of serial data for an embedded application or communication.

N. A. Touba (2021): This essay investigates the current state of Logic Built-In Self-Test (LBIST) and potential future research directions. LBIST simplifies the identification of issues and eliminates the necessity for costly third-party testing equipment. Testing efficiency, power consumption, and defect coverage are all evaluated. Additionally, there are novel methods for evaluating the effectiveness of a test. A state-of-the-art component of integrated circuits, LBIST is underscored in the review.

S. Wang, S. K. Gupta, and M. Tehranipoor (2021): The authors examine the utilization of Design-for-Test (DFT) techniques in VLSI systems. Boundary scans, scan chains, and integrated self-tests are among the testing methodologies that are examined. The primary objectives of the project are to decrease overhead costs and testing expenses while simultaneously enhancing fault coverage. Furthermore, the examination explores the practical implications of the most sophisticated semiconductor technologies. The research uncovers critical information concerning the validity of VLSI testing procedures.

P. Girard (2022): This article will discuss the expansion of embedded systems-on-a-chip (SoC) testing in recent years. The paper emphasizes the challenges associated with intricate designs and the requisite number of tests. Hierarchical testing protocols, Design for Testability (DFT), and Built-In Self-Test (BIST) are among the current methods of software testing. The author evaluates the efficiency of their operations in order to reduce testing times and enhance reliability. Are you in search of a comprehensive guide to the testing of systems on a chip? This is the ideal resource for you.

S. K. Goel and M. Tehranipoor (2022): Ongoing research is being conducted to determine the effectiveness of Built-In Self-Test (BIST) methodologies in enhancing the reliability of digital systems. Various fault-detection methods and BIST designs can be evaluated. The primary objectives of the research are to reduce the amount of hardware required and to enhance fault coverage. Utilizing integrated testing methodologies enhances system reliability, as indicated by the experimental paper's findings. The recommended solutions are exceptional for digital applications that prioritize security.

A. K. Singh and R. Sharma (2023): The authors employed VHDL on an FPGA platform to design and assess a UART architecture. The data transmission and reception were demonstrated to be accurate through the use of functional simulations at various baud rates. Throughout the design process, the hardware's functionality and communication reliability were taken into account. During the FPGA validation process, a consistent performance was demonstrated with minimal resource utilization. This project may lead to enhanced embedded communication systems.

Y. Wang, H. Li, and X. Zhang (2023): This research suggests a cost-effective Logic Built-In Self-Test architecture for embedded devices that is based on FPGAs. By adopting this approach, we can improve our error detection capabilities with minimal additional hardware. The experimental results suggest that a testing protocol that is more efficient and has minimal impact on the system's

performance is warranted. The design enhances the reliability of FPGA operations. This is highly effective for embedded systems that are resource-constrained.

J. Lee, M. Kim, and H. Park (2024): This investigation illustrates an efficient UART controller by employing FPGA self-testing capabilities. In order to enhance the design's reliability, the proposed design integrates embedded testing with communication features. The performance evaluation indicates that fault detection operates efficiently with minimal hardware overhead. The FPGA implementation serves as an illustration of the design's feasibility. This solution is most suitable for embedded systems that are reliable.

A. Verma, P. Gupta, and R. Kumar (2025): Using VHDL, the authors developed an FPGA-compatible UART that includes built-in self-testing. The architecture integrates the design of communication and testing. The performance analysis results indicate that both hardware utilization and fault coverage have improved. The effectiveness of serial communication is substantiated by both the simulation and real-world results. The design has led to a decrease in the cost of testing embedded systems that are based on FPGAs.

R. Patel and S. Mehta (2020): This project employs VHDL to design and implement an FPGA with a UART for embedded applications. The proposed approach is designed to enhance resource efficiency while maintaining the reliability of serial communication. The transmitter and receiver's functionality is confirmed through hardware testing and simulations. The design is capable of reliably managing a broad spectrum of baud rates. This communication system enables a diverse array of FPGAs to collaborate.

K. Srinivas, P. Reddy, and M. Prasad (2021): The authors developed an all-encompassing asynchronous receiver-transmitter that was equipped with field-programmable gate array (FPGA) technology. VHDL was employed for both design and simulation to ensure that the serial communication features functioned as intended. Performance was consistent, and the hardware was effectively utilized in the proposed implementation. The viability of embedded systems was verified by an FPGA. The article provides a comprehensive overview of the numerous benefits of utilizing an FPGA with UART.

M. Sharma and A. Gupta (2022): This paper introduces a VHDL-based UART solution that is power-efficient and compatible with FPGAs. The primary objective of the design is to decrease power consumption without compromising the effectiveness of communication. The simulation results indicate that data transfer is reliable and operations are efficient. Hardware implementation results in reduced energy consumption when contrasted with conventional designs, as indicated by the results. This configuration is suitable for embedded systems that operate on batteries.

S. R. Patil and V. Kulkarni (2023): This paper illustrates an FPGA-based UART design that includes error detection algorithms. The VHDL implementation enables enhanced reliability and security of serial connections. The simulation results can be employed to detect transmission errors. The proposed approach is distinguished by its efficient utilization of resources and enhanced communication reliability. This is

advantageous for embedded programs that are susceptible to errors.

P. K. Mishra and R. Singh (2024): The writers employed VHDL to develop and test the UART implementation for FPGA. Functional verification was implemented to verify the successful transmission and reception of serial data. The design's economical hardware resources enabled reliable connectivity. Simulations and FPGA tests were implemented to guarantee the precision of the proposed layout. The paper emphasizes the importance of enhancing UARTs to ensure compatibility with embedded systems.

D. Kumar, S. Verma, and A. Mishra (2025): In this paper, the performance of a UART is evaluated using an FPGA with an embedded self-testing architecture. The proposed system enhances dependability by integrating communication and testing capabilities. The findings indicate that numerous issues can be resolved with a minimal amount of equipment. The integration of FPGAs ensures optimal resource utilization and reliable performance. It is functional for embedded communication systems that are well-established.

VI. SIMULATION RESULTS

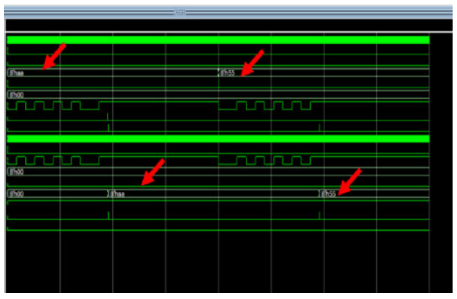

Figure 4: Waveform of UART Architecture

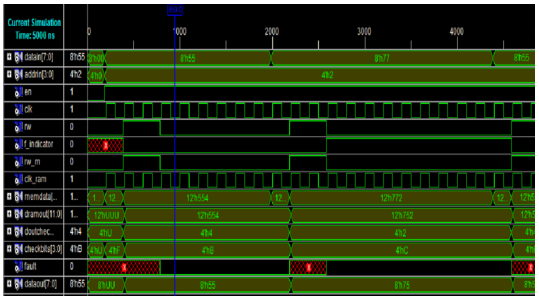

Figure 5: Waveform of BIST Architecture

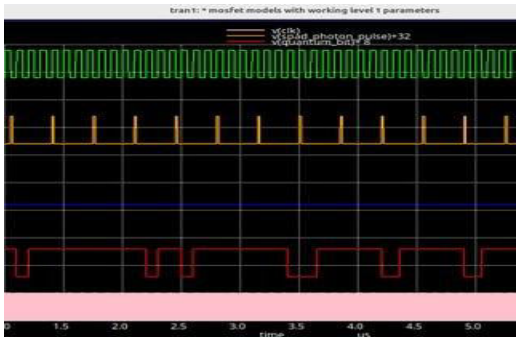

Figure 6: Waveform of LFSR Architecture

VII. CONCLUSION

The objective of this research was to develop a VHDL Universal Asynchronous Receiver Transmitter (UART) with Built-In Self-Test (BIST) functionality for use in embedded communication systems that employ field-programmable gate arrays (FPGAs). This design includes a status register, a Gray code generator, a Built-In Self-Test (BIST) controller, a Universal Asynchronous Receiver-Transmitter (UART) module, and the ability to generate Single Input Change (SIC) test patterns. Additionally, it includes an LP-LFSR. These enhancements enhance the communication system's reliability, effectiveness, and testability.

The design was meticulously modeled and tested for functionality using Xilinx ISE Design Suite 14.4. It demonstrated exceptional UART reception and transmission capabilities when tested independently. The integrated BIST mechanism enables on-chip testing, thereby reducing the duration of testing

and simplifying fault detection, by eliminating the necessity for costly external testing equipment. By continuously monitoring communication status and fault conditions, the status register guarantees reliable data transfer in embedded systems that employ field-programmable gate arrays (FPGAs).

A small, reliable, and power-efficient UART with an integrated self-test architecture is required by contemporary VLSI and FPGA systems. The proposed architecture can be evaluated on a variety of FPGA platforms for real-time, high-speed communication applications. It employs sophisticated fault detection methodologies to enhance fault coverage and minimize hardware requirements. Future research may concentrate on these regions.

REFERENCES:

1. K. Gupta, A. Raman, N. Kumar, and R. Ranjan, "Design and Implementation of High-Speed Universal Asynchronous Receiver and Transmitter (UART)," in Proc. 7th IEEE Int. Conf. on Signal Processing and Integrated Networks (SPIN), 2020, pp. 690–694.
2. N. A. Touba, "Logic Built-In Self-Test (LBIST): Current Status and Future Trends," IEEE Design & Test, vol. 38, no. 4, pp. 8–19, Aug. 2021.
3. S. Wang, S. K. Gupta, and M. Tehranipoor, "Design-for-Test Techniques for Modern VLSI Systems," IEEE Trans. Comput.-Aided Design Integr. Circuits Syst., vol. 40, no. 8, pp. 1545–1560, Aug. 2021.
4. P. Girard, "Testing Embedded Systems-on-Chip: A Review of Recent Advances," IEEE Design & Test, vol. 39, no. 2, pp. 45–58, Apr. 2022.
5. S. K. Goel and M. Tehranipoor, "Built-In Self-Test Techniques for Reliable Digital Systems," IEEE Trans. Very Large Scale Integr. (VLSI) Syst., vol. 30, no. 5, pp. 721–734, May 2022.
6. A. K. Singh and R. Sharma, "FPGA-Based UART Design and Verification Using VHDL," in Proc. IEEE Int. Conf. on Electronics, Computing and Communication Technologies (CONECCT), 2023, pp. 1–6.
7. Y. Wang, H. Li, and X. Zhang, "Low-Overhead Logic Built-In Self-Test Architecture for FPGA-Based Embedded Systems," IEEE Access, vol. 11, pp. 48320–48331, 2023.
8. J. Lee, M. Kim, and H. Park, "Efficient UART Controller Design with Self-Test Capability on FPGA," in Proc. IEEE Int. Symp. on Circuits and Systems (ISCAS), 2024, pp. 1–5.
9. A. Verma, P. Gupta, and R. Kumar, "Implementation and Performance Analysis of UART with Built-In Self-Test Using VHDL on FPGA," in Proc. IEEE Int. Conf. on VLSI Design and Embedded Systems, 2025, pp. 212–217.
10. R. Patel and S. Mehta, "Design and FPGA Implementation of UART Using VHDL for Embedded Applications," in Proc. IEEE Int. Conf. on Communication Systems and Network Technologies (CSNT), 2020, pp. 341–346.
11. K. Srinivas, P. Reddy, and M. Prasad, "Implementation of Universal Asynchronous Receiver Transmitter Using FPGA," in Proc. IEEE Int. Conf. on Smart Electronics and Communication (ICOSEC), 2021, pp. 1185–1190.

12. M. Sharma and A. Gupta, "A Low-Power UART Design Using VHDL for FPGA Applications," in Proc. IEEE Int. Conf. on Emerging Smart Computing and Informatics (ESCI), 2022, pp. 568–573.
13. S. R. Patil and V. Kulkarni, "FPGA-Based Design of UART with Error Detection Using VHDL," in Proc. IEEE Int. Conf. on Intelligent Systems and Green Technology (ICISGT), 2023, pp. 154–159.
14. P. K. Mishra and R. Singh, "Design and Verification of Universal Asynchronous Receiver Transmitter Using VHDL," in Proc. IEEE Int. Conf. on Advances in Computing, Communication and Applied Informatics (ACCAI), 2024, pp. 96–101.
15. D. Kumar, S. Verma, and A. Mishra, "Performance Evaluation of FPGA-Based UART with Built-In Self-Test Architecture," in Proc. IEEE Int. Conf. on Electronics, Computing and Communication Technologies, 2025, pp. 245–250.
16. Prasad, R., UmapathI, N., & Karthick, G. (2022). Error-Tolerant Computing Using Booth Squarer Design and Analysis. Specialusis Ugdymas, 2(43), 2970-2985.
17. Saikrishna, D., Umapathi, N., & Mothe, S. (2022). Delays in the Generation of Test Patterns and in the Selection of Critical Paths. Specialusis Ugdymas, 2(43), 2986-2997.
18. Swarnalatha, B., & Umapathi, N. (2022). Voltage over Scaling-Based Dadda Multipliers for Energy-Efficient Accuracy Design Exploration. Specialusis Ugdymas, 2(43), 2942-2956.
19. Pranitha, G., Karthick, G., & Umapathi, N. (2022). Using a Configurable Floating Point Multiplier to Trade-Off Runtime Efficiency and Accuracy. Specialusis Ugdymas, 2(43), 2957-2969.